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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/586,217 | 07/14/2006 | Johannes Dingenus Dingemanse | NL04 0062 US1 | 2771 |

65913 7590 05/29/2008

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| EXAMINER | |
|---|---|
| KERVEROS, JAMES C | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2117 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 05/29/2008 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/586,217 | DINGEMANSE, JOHANNES DINGENUS | |
| | Examiner | Art Unit | |
| | JAMES C. KERVEROS | 2117 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/14/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

This is a non-Final Office Action in response to the present US Application 10586217, filed 07/14/2006, which national stage entry of PCT/IB05/50152 international Filing Date: 01/13/2005.

Claims 1-10 are presently under examination and pending.

### *Priority*

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file, for the (EPO) Patent Application No. 04100143.9, filed 01/19/2004.

### *Drawings*

The drawings are objected to under 37 CFR 1.83(a) because they fail to show the descriptive legends associates with the functional blocks (12, 15, 20, 22, 24, 26, 61-66) for Figs. 1-6 as described in the specification. Suitable descriptive legends may be used subject to approval by the Office, or may be required by the examiner where necessary for understanding of the drawing. They should contain as few words as possible.

Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR

1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Wang et al. (US 20020184560) PGPUB DATE: December 5, 2002.

Regarding independent Claims 1, 3, 6, 7, 9, 10, Wang discloses a method and apparatus for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in a scan-based in a multiple-capture DFT (design-for-test) system, as shown in Fig. 1, including 4 clock domains (CD1 102 to CD4 105) and 4 system clocks (CK1 111 to CK4 120), each clock controlling one clock domain originally designed to run at (150, 100, 100 and 66) MHz, respectively, comprising:

a test controller (DFT system 101) arranged to switch the circuit under test (133) to a test mode (self-test or scan-test mode), wherein the DFT system 101 supplies successive test input patterns (stimuli, 109, 112, 115, 118), system

clocks (CK1 111 to CK4 120), scan enable signals (SE1 134 to SE4 137), and receives all output responses (110, 113, 116, 119). As a result, stuck-at faults within all clock domains CD1 102 to CD4 105 are detected or located during the capture cycle 202, Fig. 2.

During the shift cycle (SE), the DFT system 101 generates and shifts pseudorandom or predetermined stimuli through 109, 112, 115, and 118 to all scan cells SC in all scan chains SCN within the 4 clock domains, CD1 102 to CD4 105, simultaneously.

Then, the DFT system 101 waits until all stimuli, 109, 112, 115, and 118, have been shifted into all scan cells SC. It should be noted that, during the shift operation, the capture clock could run either at its rated clock speed (at-speed) or at a desired clock speed.

After the shift operation is completed, an ordered sequence of capture clocks is applied to all clock domains, CD1 102 to CD4 105, where each capture clock operates at its rated clock speed (at-speed) or at a slow-speed, and can be generated internally or controlled externally. In this example of Figs. 1 and 2, all system clocks, CK1 111 to CK4 120, are reconfigured to operate at a reduced frequency of 10 MHz.

After the capture operation is completed, the output responses captured into all scan cells SC are shifted out through responses 110, 113, 116, and 119 to the DFT system 101 for compaction during the compact operation in self-test mode or direct comparison during the compare operation in scan-test mode.

Fig. 2 shows a timing diagram of a full-scan design given in FIG. 1, for detecting or locating stuck-at faults within each clock domain and stuck-at faults crossing clock domains with an ordered sequence of capture clocks in self-test or scan-test mode.

Regarding Claims 2, 4, 5, 8, Wang discloses a CAD method, Fig. 33, wherein the generating HDL test benches and ATE test programs further includes transforming design database into an equivalent combinational circuit model based on the ordered sequence of capture clocks, and performing combinational ATPG (automatic test pattern generation) to generate the circuit's test patterns and report its fault coverage.

As shown in Fig. 33, the scan-based control files contain all set-up information and scripts required for design compilation 3304 to prepare a design into an internal database 3305, clock-domain analysis 3306, circuit transformation 3307 to convert the original design into an equivalent combinational circuit model 3308 corresponding to multiple time frames, selected combinational fault simulation 3309 with a selected number of pseudorandom stimuli, and selected combinational ATPG (automatic test pattern generation) 3310 to generate a plurality of scan patterns or predetermined stimuli. The combinational fault simulation can be used for self-test or scan-test, while the combinational ATPG is mainly used for scan-test.

## *Conclusion*

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques H. Louis-Jacques can be reached on (571) 272-4150. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JAMES C KERVEROS/
Primary Examiner, Art Unit 2117

Date: 28 May 2008
Office Action: Non-Final Rejection

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